IN THE CLAIMS

Please cancel claims 1-3 and 13-18.

1-3. (Canceled)

4. (Original) A method for generating timing constraints, comprising the steps of:
describing a digital circuit using a standard HDL;
constructing said digital circuit from said HDL description; and
replacing flip-flops in said digital circuit with negative delay elements.

5. (Original) The method of Claim 4, wherein said negative-time elements are implemented by buffers having a delay -T, where T is a delay equal to a flip-flop's clock period less a typical flip-flop delay.

6. (Original) The method of Claim 4, wherein if said digital circuit contains cycles, then performing the step of breaking said cycles by inserting flip-flops clocked by clocks all having a period of substantially zero.

7. (Original) The method of Claim 6, wherein cycles are only broken on backward paths.

8. (Original) The method of Claim 4, wherein clocks and registers constructed have the property of slack equivalence, wherein optimization goals at each gate are substantially the same as they would be if registers were already optimally distributed.

9. (Original) The method of Claim 5, wherein the actual value of T is set to a clock period of a flip-flop being replaced.

10. (Original) The method of Claim 4, further comprising the step of:

using a buffer to replace a flip-flop, said buffer having a typical load capacitance, representing an average or weighted-average load capacitance taken over inputs of all gates and flip-flop D pins in a target technology library.

11. (Original) The method of Claim 5, further comprising the step of:

describing a value of T using a capacitance/delay curve representing a composite of gates in a target technology library, Q pins of flip-flops in said target technology library, and a series of increasingly powerful buffer trees;

wherein said curve is first computed, then it is offset by setting a delay corresponding to typical load capacitance to –T;

whereby a larger capacitive load results in a longer delay; and

whereby if a near-zero load is imposed a delay is –(T + t), where t is a (positive) difference in delay between a typical load and a lesser load.

12. (Original) The method of Claim 4, further comprising the steps of:

after logic optimization, reinstalling registers in place of negative-delay elements;

removing all zero-clocked cycle-breaking flip-flops;

applying a retiming algorithm; and

after retiming, performing a second logic optimization pass to fine-tune said retimed design.

13-18. (Canceled)